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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,520	10/06/2003	Han-Wen Hsu	MTKP0040USA	2519

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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
03/18/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/605,520	HSU ET AL.	
	Examiner	Art Unit	
	Yolanda L. Wilson	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,12-23 and 25-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,12-23 and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims are rejected under 35 U.S.C. 102(e) as being anticipated by Ochiai (USPN 6862688B2). As per claim 1, Ochiai discloses a method for controlling a hardware circuit with a processor, the processor used for executing a code to control the hardware circuit, the code comprising:

a plurality of lower-level subroutines, wherein after the processor executes various lower-level subroutines, the hardware circuit will be controlled to execute various corresponding operations, and each lower-level subroutine will record results, which come from the hardware circuit executing the corresponding operations, in an error code; wherein each result corresponds to a recovery operation;

a plurality of higher-level subroutines, each higher-level subroutines used for calling at least a lower-level subroutine to control the hardware circuit to execute operations corresponding to the lower-level subroutine according to the called lower-level subroutine when the processor executes the higher-level subroutine;

a plurality of recovery subroutines, each recovery subroutine corresponding to a recovery operations for controlling the hardware circuit to execute various corresponding recovery operations, after the processor executes various recovery subroutines; and an error-handling subroutine for calling the recovery subroutines according to the error code;

the method comprising: after the processor executes the higher-level subroutines, executing the error-handling subroutine to allow the processor to control the hardware circuit to execute the corresponding recovery operations according to the results corresponding to the lower-level subroutines in column 7, lines 1-67.

3. As per claims 2 and 15, Ochiai discloses wherein when the processor executes the error-handling subroutine after the higher-level subroutine is executed, the processor will not execute the recovery operations corresponding to the lower-level subroutine called by the higher-level subroutine until the higher-level subroutine is finished in column 7, lines 1-67. The error handling is accomplished one section at a time.

4. As per claims 3 and 16, Ochiai discloses wherein the higher-level subroutines won't call each other so that a next higher-level subroutine will not be executed until the processor finishes executing a previous higher-level subroutine in column 7, lines 1-67. The error handling is accomplished one section at a time.

5. As per claims 6 and 19, Ochiai discloses wherein the error code is a global variable of the code; the operation results corresponding to the lower-level subroutines will be recorded in the same error code in column 7, lines 53-67.

6. As per claims 7 and 20, Ochiai discloses wherein the code further comprises a plurality of next-level subroutines; when the processor executes various next-level subroutines, the hardware circuit is controlled to execute corresponding operations; each next-level subroutines will record operation results corresponding to the hardware circuit in a second error code; each lower-level subroutine is used for calling at least a next-level subroutine so that the processor sequentially executes the next-level subroutines of the lower-level subroutines to control the hardware circuit to execute corresponding operations when executing the lower-level subroutines in column 7, lines 1-67.

7. As per claims 8 and 21, Ochiai discloses wherein the next-level subroutines of each lower-level subroutine record corresponding operation results in the same second error code in column 7, lines 1-67.

8. As per claims 9, 22, Ochiai discloses wherein the second error code is a column of the error code in column 7, lines 1-67.

9. As per claims 10 and 23, Ochiai discloses wherein the next-level subroutines record corresponding operation results in the same second error code in column 7, lines 1-67.

10. As per claims 12 and 25, Ochiai discloses wherein the lower-level subroutines won't call each other so that a new lower-level subroutine will not be executed until the processor finishes executing a previous lower-level subroutine in column 7, lines 1-67. The error handling is accomplished one section at a time.

11. As per claims 13 and 26, Ochiai discloses wherein the lower-level subroutines won't call the higher-level subroutines in column 7, lines 1-67. The error handling is accomplished one section at a time.

12. As per claims 27 and 28, Ochiai discloses wherein the error-handling subroutine unifies and manages recovery operations of all subroutines included in the program code, except the error-handling subroutine in column 7, lines 1-67.

13. As per claim 14, Ochiai discloses An electronic device, comprising: a hardware circuit for achieving operations of the electronic device; a processor for executing a code to control the hardware circuit; a storage device for storing the code ; wherein the code comprising: a plurality of lower-level subroutines, wherein after the processor executes various lower-level subroutines, the hardware circuit will be controlled to execute various corresponding operations, and each lower-level subroutine will record results, which come from the hardware circuit executing the corresponding operations, in an error code; wherein each result corresponds to a recovery operation;

a plurality of higher-level subroutines, each higher-level subroutines used for calling at least a lower-level subroutine to control the hardware circuit to execute operations corresponding to the lower-level subroutine according to the called lower-level subroutine when the processor executes the higher-level subroutine;

a plurality of recovery subroutines, each recovery subroutine corresponding to a recovery operations for controlling the hardware circuit to execute various corresponding recovery operations, after the processor executes various recovery subroutines;

and an error-handling subroutine for calling the recovery subroutines according to the error code; wherein after executing the higher-level subroutines, the processor executes the error-handling subroutine to allow the processor to control the hardware circuit to execute the corresponding recovery operations according to the results corresponding to the lower-level in column 7, lines 1-67.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4,17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Sim et al. (USPN 6785212B1). As per claim 4, 17, Ochiai fails to explicitly state wherein the hardware circuit is a servo module of an optical storage drive, the servo module comprising: a motor for driving an optical disk to rotate; and a pick-up head for generating a laser incident on the optical disk.

Sim et al. discloses these limitations in Figure 2; column 3, lines 33-47.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the hardware circuit be a servo module of an optical storage drive, the servo module comprising: a motor for driving an optical disk to rotate; and a pick-up head for generating a laser incident on the optical disk. A person of ordinary skill in the art would have been motivated to have the hardware circuit be a servo module of an optical storage drive, the servo module comprising: a motor for

driving an optical disk to rotate; and a pick-up head for generating a laser incident on the optical disk because an optical storage drive and its components read information from an optical disk which is inserted into the optical storage drive.

16. Claims 5,18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Okada et al. (USPN 6530034B1). As per claims 5,18, Ochiai fails to explicitly state wherein the hardware circuit is an interface module of an optical storage drive.

Okada et al. discloses these limitations in Figure 1; column 3, lines 3-5.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the hardware circuit be an interface module of an optical storage drive. A person of ordinary skill in the art would have been motivated to have the hardware circuit be an interface module of an optical storage drive the interface module controls when data is accessed on the storage drive. This is disclosed in column 3, lines 21-28.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda L. Wilson whose telephone number is (571) 272-3653. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Yolanda L Wilson/
Primary Examiner, Art Unit 2113